1.2.2 Number of Add on /Certificate programs offered during the year

1.2.3 Number of students enrolled in Certificate/ Add-on programs as against the total number of students during the year

Academic Year -2023-24						
Name of Add on /Certificate programs offered	Course Code (if any)	Year of offering	No. of times offered during the same year	Duration of course	Number of students enrolled in the year	Number of Students completing the course in the year
NPTEL Course on VLSI Design Flow: RTL to GDS by Electronics & Telecommunication Engg. Students		2023-24	1	July-Oct 2023 (12 weeks)	11	2

Faculty Incharge

Atma Malik Institute of Technology & Research
At.Moholi, Post-Achal, Tal-Shahapur, Dist-Thane

HOD

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Vishwatmak Jangli Maharaj Ashram Trust's

Atma Malik Institute of Technology & Research (AMRIT)

Department of Electronics & Telecommunication Engineering

Date: 12/07/2023

NPTEL Enrollment (July-Dec 2023)

Following Students have enrolled for NPTEL Course for July-Dec 2023.

Sr. No.	Name of Student	Class/Sem	NPTEL Course name	Faculty Incharge/Mentor	
1	Tushar Kadam	BE/7th Sem	VLSI Design Flow: RTL to GDS	Mr. Sumit Kumar	Pass
2	Sandesh Mhase	BE/7th Sem	VLSI Design Flow: RTL to GDS	Mr. Sumit Kumar	Pass
3	Akshata Halde	BE/7th Sem	VLSI Design Flow: RTL to GDS	Mr. Sumit Kumar	
4	Mamta Jangam	BE/7th Sem	VLSI Design Flow: RTL to GDS	Mr. Sumit Kumar	
5	Sayali Bhosale	BE/7th Sem	VLSI Design Flow: RTL to GDS	Mr. Sumit Kumar	
6	Tanvi Bhojane	BE/7th Sem	VLSI Design Flow: RTL to GDS	Mr. Sumit Kumar	
7	Swapnil Kubade	BE/7th Sem	VLSI Design Flow: RTL to GDS	Mr. Sumit Kumar	
8	Aniket Yerunkar	BE/7th Sem	VLSI Design Flow: RTL to GDS	Mr. Sumit Kumar	
9	Dinesh Kamble	TE/5th Sem	VLSI Design Flow: RTL to GDS	Mr. Sumit Kumar	
10	Karan Patil	TE/5th Sem	VLSI Design Flow: RTL to GDS	Mr. Sumit Kumar	
11	Ram Jadhav	TE/5th Sem	VLSI Design Flow: RTL to GDS	Mr. Sumit Kumar	
12	Anita Nemane	TE/5th Sem	Sensors Technology	Mr. Sumit Kumar	
13	Rituraj Kumawat	TE/5th Sem	Sensors Technology	Mr. Sumit Kumar	
14	Ram Jadhav	TE/5th Sem	Sensors Technology	Mr. Sumit Kumar	
15	Karan Patil	TE/5th Sem	Sensors Technology	Mr. Sumit Kumar	

Atma Malik Institute of Technology & Research, At-Mohili, Post-Aghai, Tal-Shahapur, Dist-Thane

Kumar

Prof. Sumit Kumar

HOD-EXTC & IQAC Coordinator

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ACAD-DI-68	**NOTICE**	Academic Year: 2023-24
Rev : 00		Semester: ODD
Date: 11-7-2022		

Date: 19/06/2023

NPTEL COURSE ENROLLMENT

Dear Learners, you are advised to take up **NPTEL online courses** and on successful completion, you are required to submit certification for the same.

Objective: This will definitely help learners to facilitate their enhanced learning based on their interest.

After successful enrollment to the NPTEL course, submit the information to your mentor.

Visit the following link to register for the course: https://docs.google.com/spreadsheets/d/e/2PACX-1vQCbGU35MAoqfECfSQCj22Kj-272L_xGjsxjgNCJWlhYn3yA25jKhX8v_NKQYffH0dSS0LquHhzhTnM/pubhtml?urp=gmail_link

Atma Malik Institute of Technology & Research, At.Maholi, Post-Asnoli, Tal-Shahapur, Dist-Thane

Prof. Sumit Kumar
HOD-EXTC & IQAC Coordinator

Dr. D. D. Shinde
Principal

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ACAD-DI-68	**NOTICE**	Academic Year: 2023-24
Rev : 00		Semester: ODD
Date: 11-7-2022		

Date: 15/09/2023

Useful VLSI courses on NPTEL

Freely available for students/faculty who are passionate about semiconductors & eager to learn.

Dear Learners, you are advised to take up **NPTEL online courses** .
These are FREE technical video lectures by faculties of IIT with decades of experience.

1. Introduction to VLSI Design:	**https://lnkd.in/gMtYBDnP**
2. Hardware modeling using Verilog:	**https://lnkd.in/gu7KnDdW**
3. System Design Through VERILOG:	**https://lnkd.in/g48RMtmJ**
4. Introduction to Digital VLSI Design Flow:	**https://lnkd.in/gqC-qUgs**
5. VLSI Physical Design:	**https://lnkd.in/gUrTSGta**
6. CAD for VLSI Design I:	**https://lnkd.in/ggmZqUJu**
7. CAD for VLSI Design II:	**https://lnkd.in/gzE4_Nqm**
8. Optimization Techniques for Digital VLSI Design:	**https://lnkd.in/gGvF4tAk**
9. Analog VLSI Design:	**https://lnkd.in/ggq7CTPX**
10. Intoduction on VLSI Design:	**https://lnkd.in/gfjTh7Gn**
11. CMOS Digital VLSI Design:	**https://lnkd.in/gbmq5vu7**
12. VLSI Design Flow - RTL to GDS:	**https://lnkd.in/gfzAfWjS**
13. VLSI Design Verification and test:	**https://lnkd.in/grJP_VgZ**
14. CMOS Analog VLSI Design:	**https://lnkd.in/g-64nBWv**
15. Semiconductor Devices:	**https://lnkd.in/gmBC_eUh**
16. Basic Electronics:	**https://lnkd.in/gAbD2gWy**
17. Digital Circuits:	**https://lnkd.in/g4_xbaCB**

Kumar

Prof. Sumit Kumar
HOD-EXTC & IQAC Coordinator

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Courses (https://swayam.gov.in/explorer) >

VLSI Design Flow: RTL to GDS

By Prof. Sneh Saurabh | IIT Delhi

Go to course (course?user_email=kumarsclab20@gmail.com) Learners enrolled: 12082 | Exam registration: 2720

VLSI Design Flow: RTL to GDS - Course Intro

ABOUT THE COURSE:
This course covers the entire RTL to GDS VLSI design flow, going through various stages of logic synthesis, verification, physical design, and testing. Besides covering the fundamentals of various design tasks, this course will develop skills in modern chip design with the help of activities and demonstrations on freely available CAD tools. This course will enhance the employability of the students and will make them ready to undertake careers in the semiconductor industry.

PREREQUISITES: Basic Course on Digital Circuits (typically taught in the first/second year of UG Program)

INDUSTRY SUPPORT: The course develops skills to use design automation tools for chip designing. The course will be valued by companies working on semiconductors, such as Qualcomm, Intel, Texas Instruments, NXP, ST Microelectronics, Micron, IBM, Cadence, Synopsys, Siemens, ARM, AMD, NVidia, Apple, and Google.

Summary

Course Status : Completed

Course Type : Elective
Duration : 12 weeks
Category : VLSI design
Credit Points : 3
Level : Undergraduate/Postgraduate
Start Date : 24 Jul 2023
End Date : 13 Oct 2023
Enrollment Ends : 07 Aug 2023
Exam Registration Ends : 18 Aug 2023
Exam Date : 29 Oct 2023 IST

Note: This exam date is subjected to change based on seat availability. You can check final exam date on your hall ticket.

This is an AICTE approved FDP course

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(https://www.addtoany.com/share#url=https%3A%2F%2Fonlinecourses.nptel.ac.in%2Fnoc23_ee137%2Fpreview&title=VLSI%20Design%20Flow%3A%20RTL%20to%20GDS%20-%20Course)

Course layout

Week 1: Basic Concepts of Integrated Circuit: Structure, Fabrication, Types, Design Styles, Designing vs. Fabrication, Economics, Figures of Merit Overview of VLSI Design Flow: Design Flows and Abstraction; Pre-RTL Methodologies: Hardware-software Partitioning, SoC Design, Intellectual Property (IP) Assembly, Behavioral Synthesis
Week 2: Overview of VLSI Design Flow: RTL to GDS Implementation: Logic Synthesis, Physical Design; Verification and Testing; Post-GDS Processes
Week 3: Hardware Modeling: Introduction to Verilog Functional verification using simulation: testbench, coverage, mechanism of simulation in Verilog
Week 4: RTL Synthesis: Verilog Constructs to Hardware Logic Optimization: Definitions, Two-level logic optimization
Week 5: Logic Optimization: Multi-level logic optimization, FSM Optimization Formal Verification: Introduction, Formal Engines: BDD, SAT Solver
Week 6: Formal Verification: Model Checking, Combinational Equivalence Checking Technology Library: Delay models of Combinational and Sequential Cells
Week 7: Static Timing Analysis: Synchronous Behavior, Timing Requirements, Timing Graph, Mechanism, Delay Calculation, Graph-based Analysis, Path-based Analysis, Accounting for Variations
Week 8: Constraints: Clock, I/O, Timing Exceptions Technology Mapping Timing-driven Optimizations
Week 9: Power Analysis, Power-driven Optimizations Design for Test: Basics and Fault Models, Scan Design Methodology
Week 10: Design for Test: ATPG, BIST Basic Concepts for Physical Design: IC Fabrication, FEOL, BEOL, Interconnects and Parasitics, Signal Integrity, Antenna Effect, LEF files
Week 11: Chip Planning: Partitioning, Floorplanning, Power Planning Placement: Global Placement, Wirelength Estimates, Legalization, Detailed Placement, Timing-driven Placement, Scan Cell Reordering, Spare Cell Placement
Week 12: Clock Tree Synthesis: Terminologies, Clock Distribution Networks, Clock Network Architectures, Useful Skews Routing: Global and Detailed, Optimizations Physical Verification: Extraction, LVS, ERC, DRC, ECO and Sign-off

Books and refere

swayam (https://swayam.gov.in/) (https://swayam.gov.in/nc_details/NPTEL)

1.Sneh Saurabh, "Introduction to VLSI Design Flow", Cambridge University Press, 2023 (expected) https://www.cambridge.org/highereducation/books/introduction-to-vlsi-design-flow/93E6832E63FE6879518 1D6D67B552334#overview (https://www.cambridge.org/highereducation/books/introduction-to-vlsi-design-flow/93E6832E63FE6879518 1D6D67B552334#overview)
2.M.J.S. Smith, "Application-specific integrated circuits", Addison-Wesley, 1997
3.L. Lavagno, I. L. Markov, G. Martin, and L. K. Scheffer (Editors), "Electronic Design Automation for IC Implementation, Circuit Design, and Process Technology", CRC Press, 2016
4.S. Palnitkar, "Verilog HDL: a guide to digital design and synthesis", Pearson Education India, 2003
5.J. Bhasker and R. Chadha, "Static timing analysis for nanometer designs: A practical approach", McGraw-Hill Higher Education, 1994
6.G. D. Michell, "Synthesis and optimization of digital circuits", McGraw-Hill Higher Education, 1994
7.M. Bushnell and V. Agrawal, "Essentials of electronic testing for digital, memory and mixed-signal VLSI circuits", Springer Science & Business Media, 2004

Instructor bio

Prof. Sneh Saurabh
IIIT Delhi

Prof.Sneh Saurabh obtained his Ph.D. from IIT Delhi in 2012 and B.Tech. (EE) from IIT Kharagpur in the year 2000. He has rich experience in the semiconductor industry, having spent 16 years working for industry leaders such as Cadence Design Systems, Synopsys India, and Magma Design Automation before joining IIIT Delhi in June 2016. He has been involved in developing some of the well-established industry-standard EDA tools for clock synchronization, constraints management, STA, formal verification, and physical design. He has taught VLSI-specific courses for over six years at IIIT Delhi, the most popular being VLSI Design Flow. His teaching has been rated excellent by students consistently, and he has received the Teaching Excellence award for seven consecutive semesters, three times for the course VLSI Design Flow. He holds three US patents and is the co-author of the book "Fundamentals of Tunnel Field-Effect Transistors." He is an Editor (IETE Technical Review), an Associate Editor (IEEE Access), a Review Editor (Frontiers in Electronics Integrated Circuits and VLSI), and a Senior Member of IEEE.

Course certificate

The course is free to enroll and learn from. But if you want a certificate, you have to register and write the proctored exam conducted by us in person at any of the designated exam centres.
The exam is optional for a fee of Rs 1000/- (Rupees one thousand only).
Date and Time of Exams: 29 October 2023 Morning session 9am to 12 noon; Afternoon Session 2pm to 5pm.
Registration url: Announcements will be made when the registration form is open for registrations.
The online registration form has to be filled and the certification exam fee needs to be paid. More details will be made available when the exam registration form is published. If there are any changes, it will be mentioned then.
Please check the form for more details on the cities where the exams will be held, the conditions you agree to when you fill the form etc.

CRITERIA TO GET A CERTIFICATE

Average assignment score = 25% of average of best 8 assignments out of the total 12 assignments given in the course.
Exam score = 75% of the proctored certification exam score out of 100

Final score = Average assignment score + Exam score

YOU WILL BE ELIGIBLE F[illegible] ONLY IF AVERAGE ASSIGNMENT SCORE >=10/25 AND EXAM SCORE >= 30/75. If one of the 2 criteria is not met, you will not ge[illegible]

swayam (https://swayam.gov.in/) (https://swayam.gov.in/nc_details/NPTEL)

Certificate will have your name, photograph and the score in it. It [illegible] with the logos of IIT/NPTEL and IIIT Delhi .It will be e-verifiable at nptel.ac.in/noc (http://nptel.ac.in/noc).

Only the e-certificate will be made available. Hard copies will not be dispatched.

Once again, thanks for your interest in our online courses and certification. Happy learning.

- NPTEL team

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Atma Malik Institute of Technology & Research
At.Moholi, Post-Aighal, Tal-Shahapur, Dist-Thane

NPTEL Online Certification

(Funded by the MoE, Govt. of India)

This certificate is awarded to

SANDESH SADANAND MHASE

for successfully completing the course

VLSI Design Flow: RTL to GDS

with a consolidated score of **52** %

Online Assignments	22.19/25	Proctored Exam	30/75

Total number of candidates certified in this course: **1877**

Dr. Anand Srivastava
Coordinator
Continued Education Program, IIITD

Jul-Oct 2023

(12 week course)

Prof. Andrew Thangaraj
NPTEL, Coordinator
IIT Madras

INDRAPRASTHA INSTITUTE of INFORMATION TECHNOLOGY DELHI

FREE ONLINE EDUCATION swayam

Roll No: NPTEL23EE137S742300672

To verify the certificate

No. of credits recommended: 3 or 4

NPTEL Online Certification

(Funded by the MoE, Govt. of India)

This certificate is awarded to

TUSHAR SARJERAO KADAM

for successfully completing the course

VLSI Design Flow: RTL to GDS

with a consolidated score of **52** %

Online Assignments	22.19/25	Proctored Exam	30/75

Total number of candidates certified in this course: **1877**

Malik Institute of Technology & Research
At.Moholi,
Dist-Thane

Jul-Oct 2023

(12 week course)

Dr. Anand Srivastava
Coordinator
Continued Education Program, IIITD

Prof. Andrew Thangaraj
NPTEL, Coordinator
IIT Madras

INDRAPRASTHA INSTITUTE of INFORMATION TECHNOLOGY DELHI

FREE ONLINE EDUCATION swayam शिक्षित भारत, उन्नत भारत

Roll No: NPTEL23EE137S742300299 To verify the certificate No. of credits recommended: 3 or 4